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ON Semiconductor Corporation and
Semiconductor Component Industries, LLC

UNITED STATES DISTRICT COURT

DISTRICT OF ARIZONA

ON Semiconductor Corporation and Semiconductor Components Industries, LLC, Delaware corporations, Plaintiffs, v. Micro Processing Technology, Inc., a California corporation, Defendant.	Case No. **COMPLAINT** **JURY TRIAL DEMANDED**

Plaintiffs ON Semiconductor Corporation and Semiconductor Components Industries, LLC for their complaint against defendant Micro Processing Technology, Inc. hereby allege and state as follows:

PARTIES

1. Plaintiffs ON Semiconductor Corporation and Semiconductor Components Industries, L.L.C. (referred to individually and collectively as "ON Semiconductor" or "Plaintiff") are Delaware corporations having their principal

place of business at 5005 East McDowell Road, Phoenix, AZ 85008. Semiconductor Components Industries, L.L.C. is the principal domestic operating subsidiary of ON Semiconductor Corporation, and does business under the name of "ON Semiconductor."

2. Upon information and belief, Defendant Micro Processing Technology, Inc. ("MPT" or "Defendant") is a California corporation with its principal place of business in Lafayette, California.

JURISDICTION AND VENUE

3. This is a civil action for correction of inventorship arising under the patent laws of the United States of America, 35 U.S.C. § 1, et seq., breach of contract, and misappropriation of trade secrets.

4. This Court has jurisdiction over the subject matter of the Complaint pursuant to 28 U.S.C. §§ 1331, 1338, & 1367.

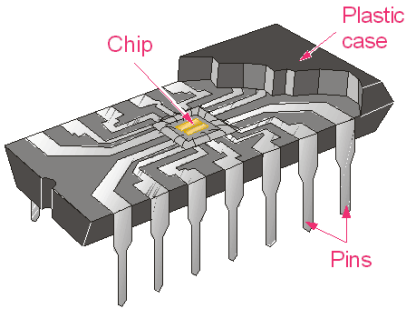
5. The Court has personal jurisdiction over MPT because, on information and belief, MPT worked with ON Semiconductor in Arizona and in California on the development of inventions that are now the subject of the complaint.

6. Venue is proper in this Judicial District under 28 U.S.C. § 1391(b) and (c) and 1400(b) because ON Semiconductor alleges Defendant has caused events to occur in Maricopa County, Arizona out of which this complaint derives.

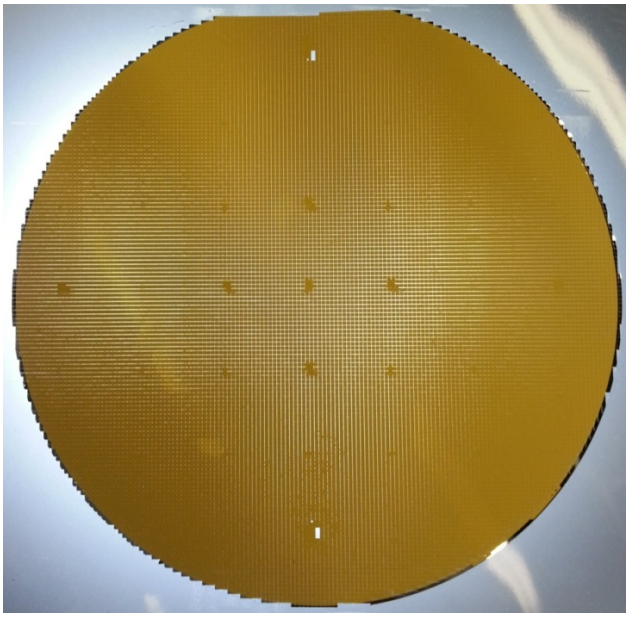
BACKGROUND

7. ON Semiconductor manufactures discrete devices and integrated circuits for use in a wide range of applications including: aerospace, automotive, LED lighting, and home entertainment. An image of one such integrated circuit is shown below:

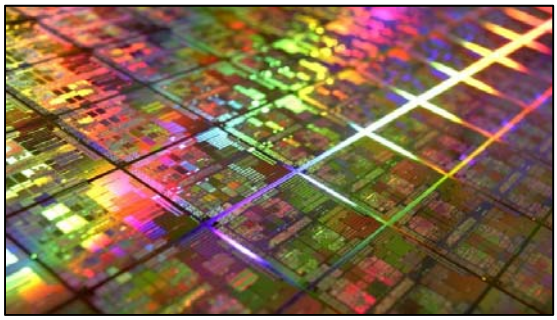
8. In general, integrated circuits, like those manufactured by ON Semiconductor, contain a single "chip" or "die" which is connected by wires to a number of "pins." The chip and pin-connections are encapsulated in a plastic case to form the packaged integrated circuit shown above. The pins allow the extremely small "chip" or "die" to be easily connected into a larger electronic system. An exploded view of an exemplary integrated circuit showing the "chip"/"die" and connected pins is shown below:



9. ON Semiconductor manufactures these individual "dies" in bulk on large platters called wafers. Wafers are usually comprised of a semiconductor substrate material which may be formed on top of a metal backing. To create individual "dies," the wafers undergo a complicated multi-step process using photo lithographic, and various doping, deposition, and etching/removal steps. These steps create thousands of copies of the same electronic circuits across a single wafer (i.e., thousands of individual dies are created on a single wafer at the same time). An exemplary 6 inch diameter wafer showing thousands of these individual tiny die, is shown below:



10. Compared to the size of the individual dies, the wafers (as can be seen above) are quite large—and can have diameters up to 16 inches, while an individual die's width is usually measured in terms of *micro*meters (one millionth of a meter). As such, a single wafer, once fully processed, can contain thousands of dies. When looking at the wafer from an aerial top down view or side view of the wafer, it looks much like a view of a city packed with skyscrapers with streets separating the skyscrapers.



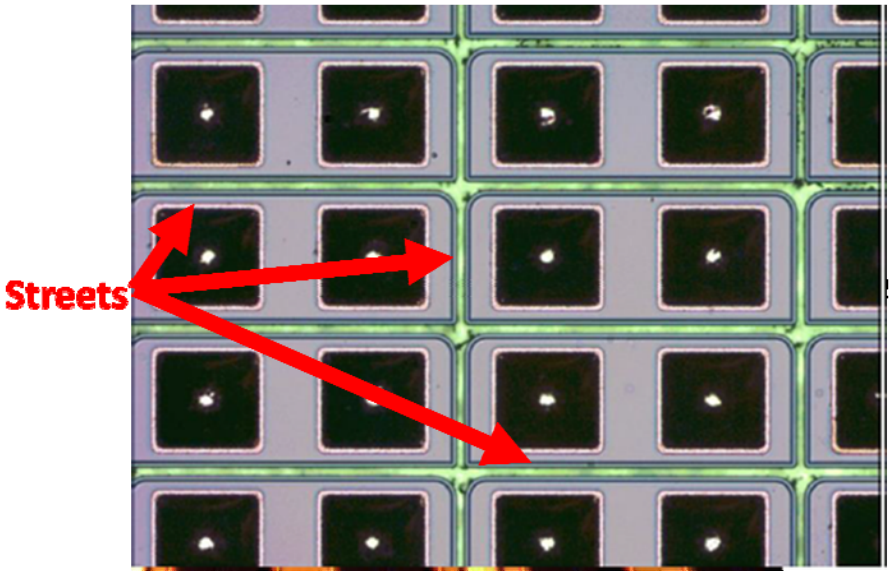
11. The individual dies typically are then separated from each other in order to be utilized.

12. The process of separating the individual dies from each other is called "dicing" or "singulation". Generally, singulation involves cutting through and/or breaking the wafer between each one of the dies. One difficulty with singulation is

that you must find a way to repeatedly and reliably separate thousands of individual dies, typically in rectangular or square shapes, without damaging them. As shown below, the dies can be smaller than a grain of salt, so great care must be taken in the singulation process so as not to damage the dies.

13. Within the wafer, the space between the dies (typically consisting of crisscross or grid pattern as shown below) is purposefully placed on the wafer to provide a space where the dies can be separated.

14. Typically, the space between the dies are often called “streets”, and, much like the streets of a city that separate the skyscrapers, the streets ensure some lateral separation between the dies on the wafer.

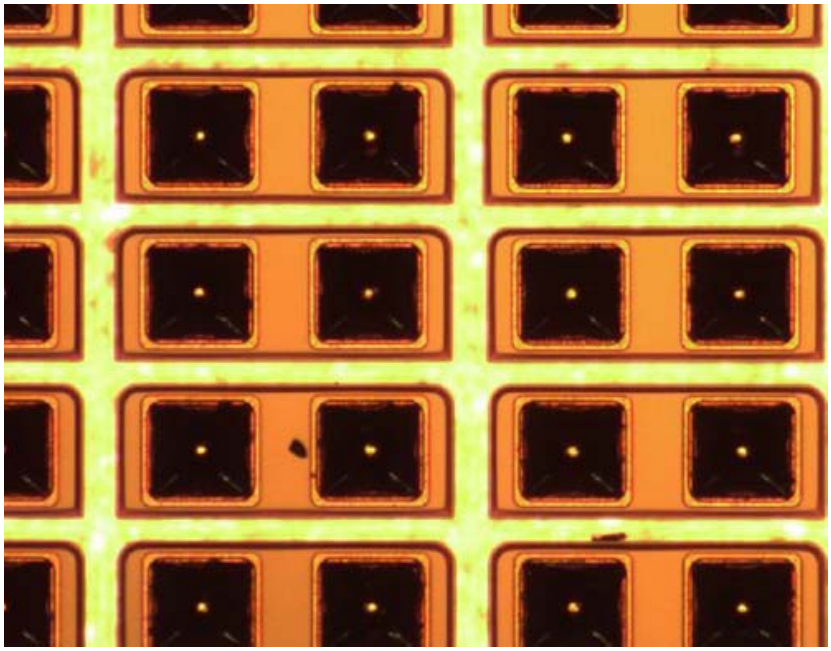


15. Typically a diamond saw is used to cut through the wafer along the streets to separate the individual dies.

16. In order to hold the individual dies in place, the wafer is typically mounted to a carrier substrate, such as adhesive tape during die singulation.

17. The dies stick to the tape while being separated from each other.

18. After the dies are singulated, the tape can then be stretched out in all directions, and the dies, which are stuck to the tape, become spread out (as shown in the image below) so that another machine can precisely pick the dies from the tape for further processing.



19. Using the sawing process, it can take up to 10 hours to singulate a single wafer containing thousands of individual dies as the cuts must be very precise due to the very small size of the streets on the wafer.

20. Prior to 2008, ON Semiconductor developed and patented a plasma etching technique ("Plasma Singulation") to replace the sawing process that significantly reduces the time it takes to singulate a single wafer. A typical Plasma Singulation process can take between 10–20 minutes to singulate the semiconductor material (e.g., silicon) between individual die on a wafer.

21. Some manufacturers of semiconductors apply a metal backing on one side of the wafer. This metal backing provides an electrical contact to the back of the silicon die which can be useful during the wafer fabrication process, but which complicates the singulation process. For example, while the sawing process removes both the silicon portion of the die and the metal backing from the streets, the Plasma Singulation process removes only the silicon portion of the die, and not the metal backing.

A. Collaboration Between ON Semiconductor and MPT

22. ON Semiconductor and MPT (collectively the "Parties") entered into a three year Confidentiality and Non-Disclosure Agreement on August 16, 2010 (the "NDA") (Exhibit 1) to work on potential solutions for removing or breaking the metal backing after Plasma Singulation in order to achieve complete die separation.

23. Beginning shortly after the Parties entered into the NDA, the Parties began experimenting with different methods to separate the metal backing. Gordon Grivna, ON Semiconductor's most decorated inventor, was involved in these collaborations on behalf of ON Semiconductor. Over the next year and a half the Parties tried to develop various methods of mechanically cutting the metal backing using a cutting wheel much like a pizza cutter ("Mechanical Cutting-Based Singulation"). Also, the parties later experimented with a different method whereby stress was applied using a stylus or roller travelling across the silicon wafer in order to cause the metal backing to break apart between the open streets ("Stylus-Based Singulation").

24. On about February 28, 2012, Gordon Grivna, conceived of the idea—alone and not in coordination with MPT—to utilize a uniform pressure differential-based stress on the wafer to facilitate metal backing singulation instead of cutting the metal backing ("Uniform Pressure Differential-Based Singulation").

25. Mr. Grivna believed having a uniform, higher pressure on one side of the wafer would cause the metal backing to fracture along the wafer's streets, breaking apart or singulating all of the die at the same time.

26. Between March and June of 2012 Mr. Grivna tested and refined this method of die separation. These tests included creating a "test fixture" to actually perform the Uniform Pressure Differential-Based Singulation method. Mr. Grivna also experimented with a hybrid design where Uniform Pressure Differential-Based Singulation and an early version of Stylus-Based Singulation were used on

the same wafer to achieve promising metal backing separation results (approximately 80% singulation). Tooling constraints with the test fixture limited the amount of additional pressure differential that could be achieved in order to realize 100% singulation.

27. On or about May 3, 2012, Mr. P.C. Lindsey of MPT visited with Mr. Grivna and other ON Semiconductor employees to discuss the latest cutting results. At that time the test fixture used in Mr. Grivna's Uniform Pressure Differential-Based Singulation experiments was assembled on the conference table just outside of Mr. Grivna's office and openly visible to Mr. Lindsey.

28. Over the months following Mr. Lindsey's visit, Mr. Grivna sent Mr. Lindsey confidential information regarding some of the methods he was exploring for solving the metal backing singulation problem, including information regarding both the Stylus-Based Singulation and the Uniform Pressure Differential-Based Singulation.

29. On July 30, 2013, ON Semiconductor and MPT entered into an Equipment Development and Proof of Concept Agreement ("P.O.C.") to further develop, build, and optimize equipment that could effect metal backing singulation. (Exhibit 2). The P.O.C. refers to this technology as a "Backmetal Cleaving System" or BCS. (*Id.*).

30. The P.O.C. expressly states that "Any Foreground Intellectual Property that is jointly developed with ON's contribution that relates to methods or processes for making semiconductor wafers or substrates (including any methods or processes jointly developed for the BCS apparatus) shall be owned by ON." (Exhibit 2, ¶ 1.1.8.5)

31. Shortly after the signing of the P.O.C., Mr. Grivna provided MPT with more detailed information regarding his Uniform Pressure Differential-Based Singulation method.

32. In addition, on August 13, 2013—before the expiration of the 2010 NDA—the Parties entered into a second, identical, three year NDA to allow them to continue to work on potential solutions for singulating metal backing layers. (Exhibit 3).

B. MPT's Surreptitious Patent Filings

33. In an email dated September 21, 2011, Mr. Lindsey requested that the Parties file "a joint patent on the back metal scribing process". However, unbeknownst to ON Semiconductor, MPT had already filed such a patent application on August 2, 2011 (which issued as U.S. Patent No. 8,450,188 (the "'188 Patent")) which claimed ownership and inventorship of a number of ideas first conceived of by ON Semiconductor's employees, including those related to Mechanical Cutting-Based Singulation. (Exhibit 4).

34. Further unbeknownst to ON Semiconductor, on January 16, 2013, MPT filed a patent application (which issued as U.S. Patent No. 9,153,493 (the "'493 Patent")) which claimed ownership and inventorship of a number of ideas first conceived of by ON Semiconductor's employees, including those related to Stylus-Based Singulation. (Exhibit 5).

35. Finally, unbeknownst to ON Semiconductor, on September 12, 2013 MPT filed a provisional patent application (which ultimately issued as U.S. Patent No. 8,906,745 (the "'745 Patent")) which also claimed ownership and inventorship of a number of ideas first conceived of by ON Semiconductor, including those related to Uniform Pressure Differential-Based Singulation. (Exhibit 6).

36. The '188 Patent expressly describes and claims a mechanical cutting-based singulation process based on concepts conceived of by ON Semiconductor and provided to Mr. Lindsey at MPT by Mr. Grivna.

37. The '188 patent names Mr. Lindsey as the sole inventor.

38. The ’493 Patent expressly describes and claims a stylus-based singulation process based on concepts conceived of by ON Semiconductor and provided to Mr. Lindsey at MPT by Mr. Grivna.

39. The ’493 patent names Mr. Lindsey as the sole inventor.

40. The ’745 Patent expressly describes and claims the Uniform Pressure Differential-Based Singulation process conceived of by ON Semiconductor and provided to Mr. Lindsey at MPT by Mr. Grivna.

41. The ’745 patent names Mr. Lindsey and a fellow MPT employee, Darrell Foote, as the only inventors.

42. The Patent Act requires, pursuant to 35 U.S.C. §§ 115 and 116, that a patent applicant identify in writing each inventor in the oath or declaration supporting a patent application.

43. On August 2, 2011, in support of the application which ultimately issued as the ’188 Patent, Mr. Lindsey executed an oath or declaration naming only Mr. Lindsey as an inventor of the ’188 Patent, to the benefit of MPT who is the named assignee of the ’188 Patent.

44. On January 16, 2013, in support of the application which ultimately issued as the ’493 Patent, Mr. Lindsey executed an oath or declaration naming only Mr. Lindsey as an inventor of the ’493 Patent, to the benefit of MPT who is the named assignee of the ’493 Patent.

45. On May 9, 2014, in support of the application which ultimately issued as the ’745 Patent, Mr. Lindsey and Mr. Darrell Foote executed an oath or declaration naming only Mr. Lindsey and Mr. Foote as inventors of the ’745 Patent, to the benefit of MPT who is the named assignee of the ’745 Patent.

46. MPT’s filings with the United States Patent and Trademark Office of Confidential Information provided by ON Semiconductor under the NDA constituted a violation of the terms of the NDA which specifically prohibit

"disclos[ing] the Confidential Information to any third party without written consent of the Discloser." (Exhibit 1, ¶3).

47. MPT's ownership claim to the intellectual property described in MPT's September 12, 2013 provisional patent application, which ultimately issued as U.S. Patent No. 8,906,745, is also a direct violation of the P.O.C. which states, "[a]ny Foreground Intellectual Property that is jointly developed with ON's contribution that relates to methods or processes for making semiconductor wafers or substrates (including any methods or processes jointly developed for the BCS apparatus) shall be owned by ON." (Exhibit 2, ¶ 1.1.8.5).

C. MPT's Attempted Enforcement of its Patent

48. On or about November 9, 2015, ON Semiconductor received a letter from MPT allegedly regarding "MPT's Intellectual Property."

49. In that letter, MPT alleged that ON Semiconductor's work to develop back-metal processing technology infringed the Parties' NDA. In particular, MPT alleged it conceived of and was the owner of the "idea of applying pressure to the tape across the entire wafer simultaneously."

50. ON Semiconductor responded on November 13, 2015, stating *inter alia*, that MPT had not provided to ON Semiconductor any confidential information related to "a whole wafer back metal cleaving solution" and, to the contrary, that ON Semiconductor had been working on its own "whole wafer back cleaving solutions with the first pressurized fluid evaluations run early 2012" and that some related Confidential Information had been shared with MPT.

51. MPT responded by letter dated November 27, 2015, and for the first time referred to "MPT's patented process" and described that process as a "patented MPT invention that utilizes a fluid pressure to apply uniform pressure across the entire wafer." MPT further alleged that ON Semiconductor's work with a third-party potentially infringed MPT's "patented process" and demanded that

ON Semiconductor "CEASE AND DESIST [ITS] USE OF MPT'S PATENTS AND/OR TRADE SECRETS."

52. ON Semiconductor first became aware of the existence of the '745 Patent in late 2015, shortly before ON Semiconductor received the letters from MPT. After ON Semiconductor received the letters from MPT, ON Semiconductor reviewed the '745 patent in detail and realized that the patent claimed to cover material which was originally invented by ON Semiconductor.

53. ON Semiconductor first became aware of the existence of the '493 Patent and realized that it claimed to cover material which was originally invented by ON Semiconductor shortly after the '493 Patent became the subject of litigation between MPT and a third-party company (on or about December of 2015).

54. ON Semiconductor first became aware of the existence of the '188 Patent within the past two months and only then realized that it claimed to cover material which was originally invented by ON Semiconductor.

55. At the same time ON Semiconductor learned of each of these patents, ON Semiconductor learned that MPT had filed for patent applications covering technology invented in whole or in part by ON Semiconductor and that MPT had failed to inform the United States Patent Office that ON Semiconductor's employee(s) should be co-inventor(s) of the '188, '493, and '745 Patents.

56. Reviewing the issued patents, ON Semiconductor also learned at that time that MPT had disclosed in the patent applications information marked as Confidential Information under the NDAs in violation of the NDAs.

57. ON Semiconductor also learned at that time that MPT had breached the P.O.C. by not assigning to ON Semiconductor the '745 Patent which, under the terms of the P.O.C. was jointly developed and relates to "a method or process jointly developed for the BCS apparatus" and, thus, "shall be owned by [ON Semiconductor]."

COUNT I
(Correction of Inventorship of '745 Patent)

58. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–57, as if fully set forth herein.

59. This is a cause of action pursuant to 35 U.S.C. § 256 to correct the inventorship of the '745 Patent.

60. The '745 Patent issued on December 9, 2014.

61. The '745 Patent names Paul C. Lindsey, Jr. and Darrell Foote as the sole inventors.

62. Upon information and belief, Mr. Lindsey, Mr. Foote, and/or MPT through innocent omission and/or oversight, failed to name Mr. Grivna, who contributed to the conception of one or more claims, as a joint inventor in the '745 Patent.

63. By failing to name Mr. Grivna as a joint inventor in the declaration filed on May 9, 2014 in support of the application which ultimately issued as the '745 Patent, Mr. Lindsey, Mr. Foote, and/or MPT violated 35 U.S.C. §§ 115 and 116, which require the identification of each inventor in the oath or declaration supporting a patent application.

64. Without correction of the named inventors under 35 U.S.C. § 256, Mr. Lindsey, Mr. Foote, and/or MPT's violation of these federal statutes will continue unabated to the detriment of Mr. Grivna and the public at large.

65. ON Semiconductor therefore, requests correction of the inventors named in the '745 Patent to insure compliance with the federal requirements for filing patent applications and to properly identify the inventors for the benefit of the public.

COUNT II
(Correction of Inventorship of '493 Patent)

66. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–65, as if fully set forth herein.

67. This is a cause of action pursuant to 35 U.S.C. § 256 to correct the inventorship of the '493 Patent.

68. The '493 Patent issued on October 6, 2015.

69. The '493 Patent names Paul C. Lindsey as the sole inventor.

70. Upon information and belief, Mr. Lindsey and/or MPT through innocent omission and/or oversight, failed to name Mr. Grivna, who contributed to the conception of one or more claims, as a joint inventor in the '493 Patent.

71. By failing to name Mr. Grivna as a joint inventor in the declaration filed on January 16, 2013 in support of the application which ultimately issued as the '493 Patent, Mr. Lindsey and/or MPT violated 35 U.S.C. §§ 115 and 116, which require the identification of each inventor in the oath or declaration supporting a patent application.

72. Without correction of the named inventors under 35 U.S.C. § 256, Mr. Lindsey and/or MPT's violation of these federal statutes will continue unabated to the detriment of Mr. Grivna and the public at large.

73. ON Semiconductor therefore, requests correction of the inventors named in the '493 Patent to insure compliance with the federal requirements for filing patent applications and to properly identify the inventors for the benefit of the public.

COUNT III
(Correction of Inventorship of '188 Patent)

74. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–73, as if fully set forth herein.

75. This is a cause of action pursuant to 35 U.S.C. § 256 to correct the inventorship of the ’188 Patent.

76. The ’188 Patent issued on May 28, 2013.

77. The ’188 Patent names Paul C. Lindsey as the sole inventor.

78. Upon information and belief, Mr. Lindsey and/or MPT through innocent omission and/or oversight, failed to name Mr. Grivna, who contributed to the conception of one or more claims, as a joint inventor in the ’188 Patent.

79. By failing to name Mr. Grivna as a joint inventor in the declaration filed on August 2, 2011 in support of the application which ultimately issued as the ’188 Patent, Mr. Lindsey and/or MPT violated 35 U.S.C. §§ 115 and 116, which require the identification of each inventor in the oath or declaration supporting a patent application.

80. Without correction of the named inventors under 35 U.S.C. § 256, Mr. Lindsey and/or MPT’s violation of these federal statutes will continue unabated to the detriment of Mr. Grivna and the public at large.

81. ON Semiconductor therefore, requests correction of the inventors named in the ’188 Patent to insure compliance with the federal requirements for filing patent applications and to properly identify the inventors for the benefit of the public.

COUNT IV
(Breach of Contract re: NDA and ’493 Patent)

82. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–81 as if fully set forth herein.

83. On January 16, 2013, MPT filed a patent application which ultimately issued as the ’493 Patent.

84. Prior to the filing of the ’493 Patent, on August 16, 2010 the parties entered into a written NDA.

85. ON Semiconductor performed its obligations under the NDA.

86. The NDA, entered into by the parties, expressly prohibits "disclos[ing] the Confidential Information to any third party without written consent of the Discloser." (Exhibit 1, ¶3).

87. The specification and claims of the '493 Patent which were submitted to the United States Patent Office included information which ON Semiconductor had designated as its Confidential Information pursuant to the NDA.

88. ON Semiconductor did not give MPT permission to disclose this information to any third-parties.

89. By disclosing ON Semiconductor's Confidential Information to the Patent Office and also causing such information to be publicly published through the issuance of the '493 Patent on October 6, 2015, MPT has materially breached the terms of the NDA.

90. In the NDA, the Parties agreed that the "improper disclosure of Confidential Information may be irreparable."

91. Due to MPT's breach of the NDA, ON Semiconductor has suffered irreparable harm and continues to suffer damages due to its Confidential Information being publicly available to competitors.

92. ON Semiconductor is entitled to recover damages caused by MPT's breach of contract.

93. Pursuant to A.R.S. § 12-341.01, this cause of action arises out of a contract and ON Semiconductor is entitled to recover its attorney's fees in addition to damages.

COUNT V
(Breach of Contract re: NDA and '745 Patent)

94. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–93 as if fully set forth herein.

95. On September 12, 2013, MPT filed a provisional patent application which ultimately issued as the '745 Patent.

96. Prior to the filing of the '745 Patent, on August 16, 2010 the parties entered into a written NDA.

97. In addition, prior to the filing of the '745 Patent, on August 13, 2013 the Parties entered into a second, identical, three year NDA.

98. ON Semiconductor performed its obligations under the NDAs.

99. The written NDAs, entered into by the parties, expressly prohibits "disclos[ing] the Confidential Information to any third party without written consent of the Discloser." (Exhibit 1, ¶3).

100. The specification and claims of the '745 Patent and the information in the provisional patent application which was submitted to the United States Patent Office included information which ON Semiconductor had designated as its Confidential Information pursuant to the NDAs.

101. ON Semiconductor did not give MPT permission to disclose this information to any third-parties.

102. By disclosing ON Semiconductor's Confidential Information to the Patent Office and also causing such information to be publicly published through the issuance of the '745 Patent on December 9, 2014, MPT has materially breached the terms of the NDAs.

103. In the NDAs, the Parties agreed that the "improper disclosure of Confidential Information may be irreparable."

104. Due to MPT's breach of the NDA, ON Semiconductor has suffered irreparable harm and continues to suffer damages due to its Confidential Information being publicly available to competitors.

105. ON Semiconductor is entitled to recover damages caused by MPT's breach of contract.

106. Pursuant to A.R.S. § 12-341.01, this cause of action arises out of a contract and ON Semiconductor is entitled to recover its attorney's fees in addition to damages.

COUNT IV
(Breach of Contract re: NDA and '188 Patent)

107. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–106 as if fully set forth herein.

108. On August 2, 2011, MPT filed a patent application which ultimately issued as the '188 Patent.

109. Prior to the filing of the '188 Patent, on August 16, 2010 the parties entered into a written NDA.

110. ON Semiconductor performed its obligations under the NDA.

111. The NDA, entered into by the parties, expressly prohibits "disclos[ing] the Confidential Information to any third party without written consent of the Discloser." (Exhibit 1, ¶3).

112. The specification and claims of the '188 Patent which were submitted to the United States Patent Office included information which ON Semiconductor had designated as its Confidential Information pursuant to the NDA.

113. ON Semiconductor did not give MPT permission to disclose this information to any third-parties.

114. By disclosing ON Semiconductor's Confidential Information to the Patent Office and also causing such information to be publicly published through the issuance of the '188 Patent on May 28, 2013, MPT has materially breached the terms of the NDA.

115. In the NDA, the Parties agreed that the "improper disclosure of Confidential Information may be irreparable."

116. Due to MPT's breach of the NDA, ON Semiconductor has suffered irreparable harm and continues to suffer damages due to its Confidential Information being publicly available to competitors.

117. ON Semiconductor is entitled to recover damages caused by MPT's breach of contract.

118. Pursuant to A.R.S. § 12-341.01, this cause of action arises out of a contract and ON Semiconductor is entitled to recover its attorney's fees in addition to damages.

COUNT V
(Breach of Contract re: P.O.C. and '745 Patent)

119. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–118 as if fully set forth herein.

120. On September 12, 2013, MPT filed a provisional patent application which ultimately issued as the '745 Patent.

121. On July 30, 2013 the parties entered into a written Proof of Concept Agreement ("P.O.C.").

122. ON Semiconductor performed its obligations under the P.O.C.

123. The written P.O.C., entered into by the parties, expressly states that "Background Intellectual Property" which is "owned or controlled" by a party prior to the effective date "shall remain with such Party." (Exhibit 2, ¶¶ 1.1.8.1 and 1.1.8.5).

124. The written P.O.C., entered into by the parties, expressly states that "Foreground Intellectual Property that is jointly developed with ON's contribution . . . including any methods or processes jointly developed for the BCS apparatus[] shall be owned by ON."

125. The specification and claims of the '745 Patent and the information in the provisional patent application which was submitted to the United States Patent

Office included methods for backside metal separation which ON Semiconductor developed prior to and during the term of the P.O.C. and shared with MPT "for the BCS apparatus", as such whether characterized as "Background" or "Foreground" Intellectual Property, those methods belong to ON Semiconductor.

126. The invention(s) described in the specification and claims of the '745 Patent constitute, at best, a "method" created through ON Semiconductor and MPT joint development for the BCS apparatus; and, as such, the '745 Patent belongs to ON Semiconductor under the terms of the P.O.C. At worst, the invention(s) described in the specification and claims of the '745 Patent constitutes ON Semiconductor's sole independently-developed Background Intellectual Property and as such belongs to ON Semiconductor under the terms of the P.O.C.

127. ON Semiconductor never assigned its ownership or other rights in the invention(s) described in the specification and claims of the '745 Patent to MPT.

128. By asserting ownership of the '745 Patent and the intellectual property described therein, and by not assigning the '745 Patent to ON Semiconductor, MPT has materially breached the terms of the P.O.C.

129. Due to MPT's breach of the P.O.C., ON Semiconductor has suffered irreparable harm and continues to suffer damages due to MPT's assertions of patent infringement as described in its November 27, 2015 letter.

130. In addition, pursuant to the Parties' agreement, ON Semiconductor is entitled to the equitable relief of obtaining ownership of the '745 Patent.

131. ON Semiconductor is entitled to recover damages caused by MPT's breach of contract.

132. Pursuant to A.R.S. § 12-341.01, this cause of action arises out of a contract and ON Semiconductor is entitled to recover its attorney's fees in addition to damages.

COUNT VI
(Misappropriation of Trade Secrets)

133. ON Semiconductor repeats and re-alleges the allegations in preceding paragraphs 1–132 as if fully set forth herein.

134. During the term of the NDAs, ON Semiconductor shared Confidential Information with MPT which ON Semiconductor considered to be its trade secret information.

135. This information, including, *inter alia*, ON Semiconductor's methods for (1) using a stylus to cause the back metal in the scribe streets to separate, and (2) using Uniform Pressure Differential-Based Singulation constituted trade secret information.

136. This information was not publicly available at the time of its disclosure, and ON Semiconductor marked documents containing this information "ON Semiconductor Confidential."

137. The advantages provided by this information provide ON Semiconductor with a real economic advantage over its competitors, including the ability of ON Semiconductor to manufacture integrated circuits at a reduced cost and increased speed.

138. At all times, ON Semiconductor took reasonable efforts to maintain the secrecy of this information, including not sharing any of this information with MPT prior to MPT signing the NDA and agreeing to not disclose ON Semiconductor's Confidential Information.

139. MPT's disclosure and claim of ownership of this intellectual property constitutes a misappropriation of ON Semiconductor's trade secrets.

140. Mr. Lindsey is MPT's President, and as such, both Mr. Lindsey and MPT knew that the methods which they represented to the USPTO were invented by Mr. Lindsey, Mr. Foote or MPT were really the intellectual property of ON Semiconductor.

141. Due to MPT's misappropriation of ON Semiconductor's trade secrets, ON Semiconductor has suffered irreparable harm through the public disclosure of ON Semiconductor's trade secrets.

142. In addition, ON Semiconductor continues to suffer damages due to MPT's assertions of ownership of ON Semiconductor's trade secrets and intellectual property as described in its November 27, 2015 letter.

143. ON Semiconductor is entitled to recover damages caused by MPT's misappropriation.

PRAYER FOR RELIEF

WHEREFORE, ON Semiconductor prays that judgment be entered by this Court in its favor and against MPT as follows:

1. Inventorship of the '745, '493, and '188 Patents be corrected pursuant to 35 U.S.C. § 256.

2. ON Semiconductor be awarded the equitable relief of sole ownership of the '745, '493, and '188 Patents.

3. ON Semiconductor be awarded damages in an amount to be proven at trial to compensate ON Semiconductor for MPT's breach of the NDAs.

4. ON Semiconductor be awarded damages in an amount to be proven at trial to compensate ON Semiconductor for MPT's breach of the P.O.C.

5. ON Semiconductor be awarded damages in an amount to be proven at trial to compensate ON Semiconductor for MPT's misappropriation of ON Semiconductor's trade secrets.

6. ON Semiconductor be awarded its attorney's fees pursuant to A.R.S. § 12-341.01.

7. That ON Semiconductor be granted such other and further relief as the Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiff ON Semiconductor hereby demands a jury trial as to all issues that are so triable.

Respectfully submitted,

QUARLES & BRADY LLP

Dated: April 14, 2016

/s/ Gregory P. Sitrick

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CERTIFICATE OF SERVICE

I hereby certify that on April 14, 2016, I electronically filed the foregoing with the Clerk of Court using the CM/ECF system, which will send a notification of such filing to all counsel of record in this case.

/s/ Gregory P. Sitrick
Gregory P. Sitrick